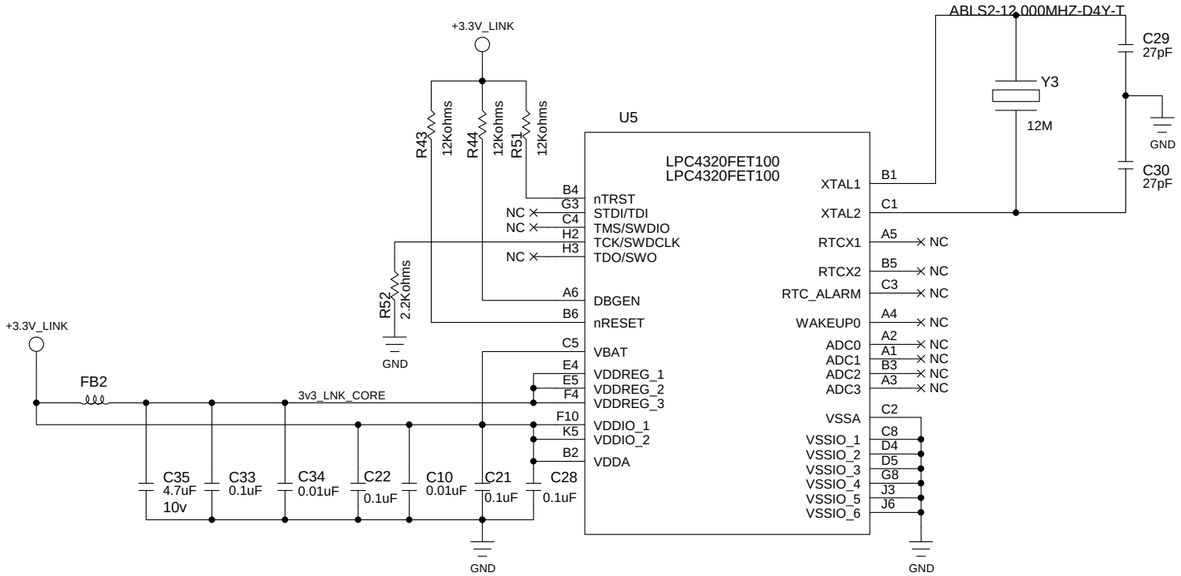
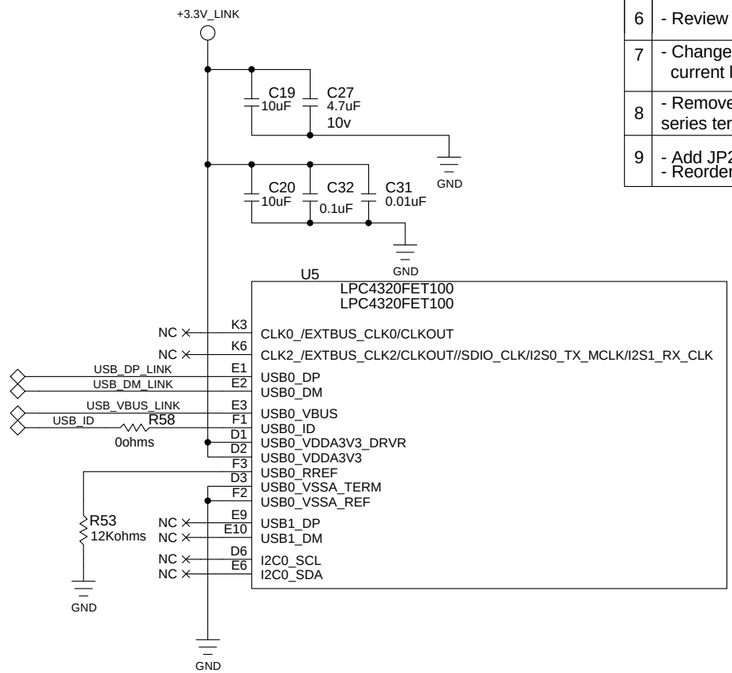
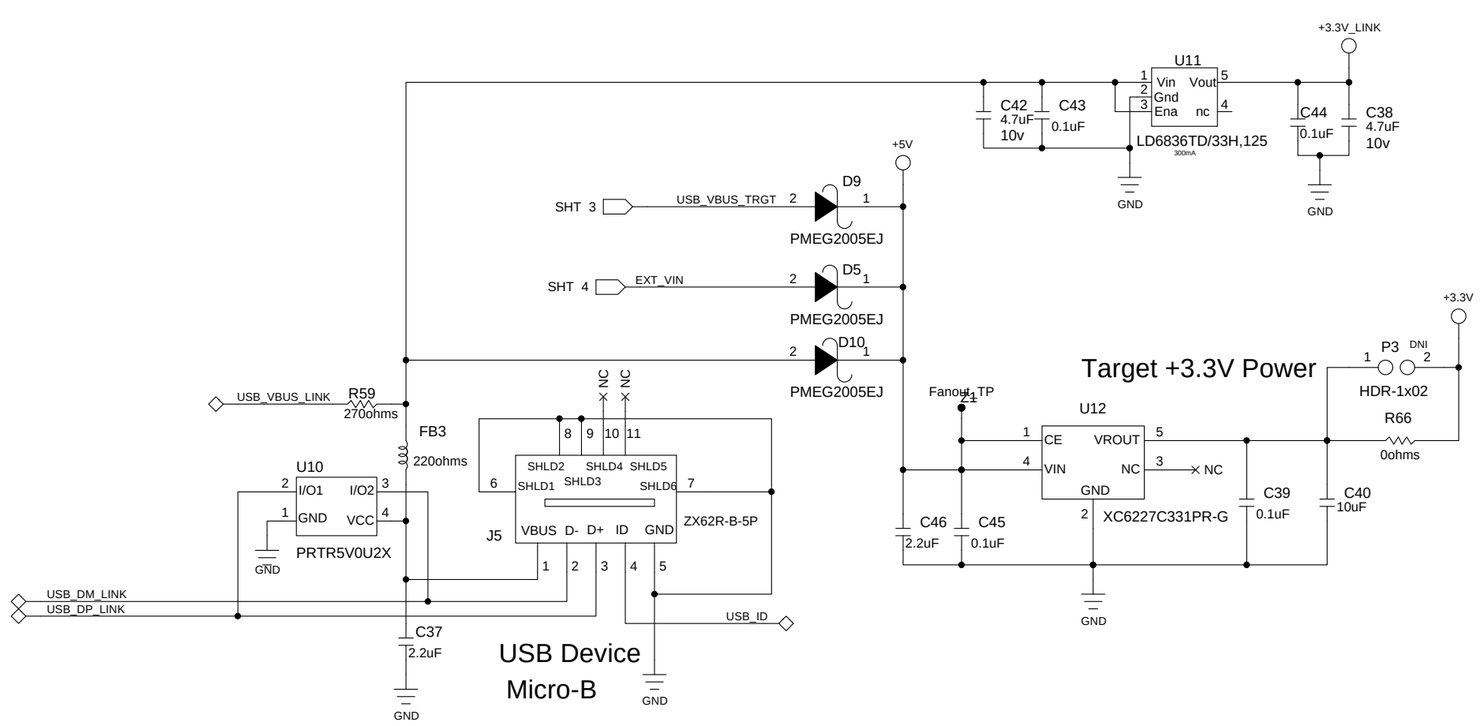
DWG. NO.	SH.	REV
Xpresso-LPC15xx	1	9

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
6	- Review	08/20/2013	
7	- Changed SWD interface / LPC1549 current limit Res to 100ohm.	08/28/2013	
8	- Removed LPC1549 USB D+/D- series termination resistors	09/01/2013	
9	- Add JP2 to force Link DFU boot. - Reorder reference designators.	09/05/2013	







CONTRACT NO.		LINK LPC4320		
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN d.consiglio	9/5/2013			
CHECKED				
ISSUED	9/05/13	SIZE D	FSCM NO.	DWG. NO. Xpresso-LPC15xx REV 9
		SCALE		SHEET 1 OF 04

H:8ND; V:4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U5
LPC4320FET100
LPC4320FET100

TRACE_D0 G2 — P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
TRACE_D1 G1 — P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1
NC H1 — P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
BOOT0_LED K2 — P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
BOOT1 K1 — P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
NC J1 — P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
NC J2 — P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
TMS_SWDIO_TXEN J4 — P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
TMS_SWDIO K4 — P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
NC G4 — P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
NC H5 — P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
NC J5 — P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
NC H6 — P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
NC J7 — P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
TRACE_CLK K7 — P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
NC H8 — P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
TDO_SWO J8 — P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
TRACE_D2 K8 — P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
TRACE_D3 H9 — P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
TCK_SWCLK H10 — P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
JTAG_TDI J10 — P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
NC K9 — P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
NC K10 — P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

U5
LPC4320FET100
LPC4320FET100

TARGET_UART_RXD G10 — P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
TARGET_UART_TXD G7 — P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
TARGET_UART_CTRL F5 — P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
ISP_CTRL D8 — P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
D9 — P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
NC D10 — P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
JTAG_RESET G9 — P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
BOOT_FLASH C10 — P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
BOOT2 C6 — P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
BOOT3 B10 — P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
E8 — P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
NC A9 — P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
NC B9 — P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
IF_DETECT — R14 1.5Kohms — NC A10 — P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4
A8 — P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
NC F7 — P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
NC G6 — P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
NC A7 — P3[3]_//SPI_SCK/SSP0_SCK/SPIFI_SCK
NC B8 — P3[4]_/GPIO1[14]///SPIFI_SIO3
NC B7 — P3[5]_/GPIO1[15]///SPIFI_SIO2
NC C7 — P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
NC D7 — P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
NC E7 — P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

U5
LPC4320FET100
LPC4320FET100

NC H7 — P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
NC G5 — P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
J9 — P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
F6 — P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
NC F9 — P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
F8 — P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
C9 — P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
NC H4 — PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

R45 DNI 2.2Kohms, R33 DNI 2.2Kohms, R34 DNI 2.2Kohms, R32 2.2Kohms — GND

+3.3V_LINK

R42 DNI 2.2Kohms, R26 2.2Kohms, R28 DNI 2.2Kohms, R30 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R41 2.2Kohms, R25 DNI 2.2Kohms, R27 2.2Kohms, R29 DNI 2.2Kohms
R31 2.2Kohms
BOOT_FLASH — JP2 HDR-1x02
D2 LS Q976-NR-1
GND

LPC4320 Boot mode
DFU USB0 = B3:0 = 0101

Short JP2 to force DFU boot
(when internal flash is programmed)

+3.3V_LINK

U4
SN74AVC2T45DCTR
SN74AVC2T45DCTR
VCCA, VCCB, A0, B0, A1, B1, DIR, GND

TCK_SWCLK, JTAG_TDI
R35 100ohms — IF_SWCLK
R36 100ohms — IF_JTAG_TDI
C11 0.1uF — GND

+3.3V
D1 PMEG1020EJ
JP1 HDR-1x02

U6
74LVC1T45GW
TDO_SWO — IF_SWO
C14 0.1uF
R47 100Kohms

U8
74LVC1T45GW
TMS_SWDIO — R55 100ohms — IF_SWDIO
C15 0.1uF
R54 100Kohms

U1
74LVC1T45GW
JTAG_RESET — R2 100ohms — IF_RST
C1 0.1uF
R1 100Kohms

TMS_SWDIO_TXEN — R56 2.2Kohms
JTAG_RESET_TXEN — R3 2.2Kohms

+3.3V_LINK
U2 74LVC1G07GW
ISP_CTRL — R4 100ohms — IF_ISPEN

C3 10uF
P1 FTSH-105-01-L-DV-K
IF_SWDIO, IF_SWCLK, IF_SWO, IF_JTAG_TDI, IF_RST

Target (LPC15xx)
SWD Debug

+3.3V
R6 0ohms
IF_SWDIO — R18 0ohms — SWDIO-PIO0_20 — SHT 3
IF_SWCLK — R16 0ohms — SWCLK-PIO0_19 — SHT 3
IF_RST — R17 0ohms — RESET-PIO0_21 — SHT 3, 4
IF_ISPEN — R15 0ohms — PIO1_10-RS485_RTS — SHT 3, 4
IF_DETECT — R5 0ohms

Remove resistors to
dissconnect target MCU

TRACE_CLK — R11 DNI 0ohms — NC
TRACE_D0 — R10 DNI 0ohms — NC
TRACE_D1 — R9 DNI 0ohms — NC
TRACE_D2 — R12 DNI 0ohms — NC
TRACE_D3 — R13 DNI 0ohms — NC

LPC1549 Target
does not have trace.

+3.3V
U9 74LVC1G3157GW
TARGET_UART_CTRL — SEL
SHT 4 — ISP_RX — Y0
TARGET_UART_RXD — Y1
Z — TO_MUX_ISP_RX — SHT 3
R57 2.2Kohms — GND

TARGET_UART_TXD — R46 100ohms — ISP_TX — SHT 3, 4

CONTRACT NO.		LINK LPC4320	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	9/5/2013		
CHECKED			
ISSUED	9/05/13	SIZE D / FSCM NO. / DWG. NO. Xpresso-LPC15xx / REV 9	
		SCALE / SHEET 2 OF 04	

H:8ND; V:4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

USB Device Micro-B

J3 ZX62R-B-5P — SHLD5 SHLD4 SHLD2 SHLD6 SHLD3 SHLD1 — GND ID D+ D- VBUS

NC NC NC

PIO1_11-ISP_1 — SJ1 — PIO0_16

R50 470ohms

U3 PRTR5V0U2X — I/O2 I/O1 VCC GND

C13 0.1uF

R40 2.2Kohms

SHT 1 USB_VBUS_TRGT

RESET-PIO0_21

USB_DM

USB_DP

SHT 4 PIO0_17-OLED_EN

SHT 2 SWCLK-PIO0_19

SHT 2 SWDIO-PIO0_20

U7

LPC1549JBD64
LPC1549JBD64

nRESET/PIO0_21 (45)
USB_DM (48)
USB_DP (47)
PIO0_17/WAKEUP/nTRST (39)
SWCLK/PIO0_19/TCK (40)
SWDIO/PIO0_20/SCT1_OUT6/TMS (44)

VSS_1 (56) VSS_2 (26) VSS_3 (27) VSS_4 (55)

VREFN (14) VSSA (21)

XTALIN (36) XTALOUT (35) RTCXIN (42) RTCXOUT (43)

VDD_1 (22) VDD_2 (52) VDD_3 (37) VDD_4 (57)

VREFP (13) VDDA (20) VDDCMP (18) VBAT (41)

ABLS2-12.000MHZ-D4Y-T — Y2 12M — C5 27pF — C6 27pF — GND

SSPT7F-7PF20-R — Y1 32.768k — C2 5pF 50V 5% — C4 5pF 50V 5% — GND

R8 100Kohms

+3.3V

C25 0.1uF C18 0.01uF C12 0.1uF C16 0.01uF C9 0.1uF C8 0.01uF C23 0.1uF C17 0.01uF

FB1

+3.3VA — C24 0.1uF — C36 10uF — GND

+3.3VBAT — C7 0.1uF — GND

D4 1N4448WS-7-F

D3 1N4448WS-7-F — VBAT — SHT 4

+3.3V — R68 12Kohms — R67 2.2Kohms — D6 (Red) LS Q976-NR-1

SHT 2, 4 RESET-PIO0_21 — C41 0.1uF — GND

+3.3V — R20 2.2Kohms — R19 2.2Kohms

U7

LPC1549JBD64
LPC1549JBD64

SHT 4	PIO0_0-SCT0_OUT3-RED	2	PIO0_0/ADC0_10/SCT0_OUT3
SHT 4	PIO0_1-SCT0_OUT4-BLUE	5	PIO0_1/ADC0_7/SCT0_OUT4
SHT 4	PIO0_2-SCT1_OUT3	6	PIO0_2/ADC0_6/SCT1_OUT3
SHT 4	PIO0_3-SCT1_OUT4	7	PIO0_3/ADC0_5/SCT1_OUT4
SHT 4	PIO0_4-ADC0_4	8	PIO0_4/ADC0_4
SHT 4	PIO0_5-ADC0_3	9	PIO0_5/ADC0_3
SHT 4	PIO0_6-SCT0_OUT0	10	PIO0_6/ADC0_2/SCT2_OUT3
SHT 4	PIO0_7-ADC0_1	11	PIO0_7/ADC0_1
SHT 4	PIO0_8-ADC0_0	12	PIO0_8/ADC0_0/TDO
SHT 4	PIO0_9-ADC1_1	16	PIO0_9/ADC1_1/TDI
SHT 4	PIO0_10-ADC1_2	19	PIO0_10/ADC1_2
	PIO0_11-CAN_RD	23	PIO0_11/ADC1_3
SHT 4	PIO0_12-AIN_CTRL	24	PIO0_12/DAC_OUT
SHT 4	PIO0_13-ISP_RX	29	PIO0_13/ADC1_6

	PIO0_14/ADC1_7/SCT1_OUT5	30	PIO0_14
	PIO0_15/ADC1_8	31	PIO0_15
	PIO0_16/ADC1_9	32	PIO0_16 — SHT 4
	PIO0_18/SCT0_OUT5	17	PIO0_18-ISP_TX
	PIO0_22/I2C0_SCL	49	PIO0_22-I2C_SCL
SHT 4	PIO0_23/I2C0_SDA	50	PIO0_23-I2C_SDA
SHT 4	PIO0_24/SCT0_OUT6	58	PIO0_24-SCT0_OUT6-GREEN
SHT 4	PIO0_25/ACMP0_I4	60	PIO0_25-BREAK_CTRL
SHT 4	PIO0_26/ACMP0_I3/SCT3_OUT3	61	PIO0_26-SCT0_OUT2
SHT 4	PIO0_27/ACMP_I1	62	PIO0_27-CURR_TRIP
SHT 4	PIO0_28/ACMP1_I3	63	PIO0_28-CURR_TRIP_RST
SHT 4	PIO0_29/ACMP2_I3/SCT2_OUT4	64	PIO0_29-SCT0_OUT1
SHT 4	PIO0_30/ADC0_11	1	PIO0_30-BREAK_STS1
	PIO0_31/ADC0_9	3	PIO0_31-CAN_TD

PIO0_15 — R37 0ohms — BREAK_STS0 — SHT 4

U7

LPC1549JBD64
LPC1549JBD64

SHT 4	PIO1_0-QEI	4	PIO1_0/ADC0_8
SHT 4	PIO1_1-QEI	15	PIO1_1/ADC1_0
SHT 4	PIO1_2-QEI	25	PIO1_2/ADC1_4
SHT 4	PIO1_3-ADC1_5	28	PIO1_3/ADC1_5
SHT 4	PIO1_4-JOY_U	33	PIO1_4/ADC1_10
SHT 4	PIO1_5-JOY_C	34	PIO1_5/ADC1_11
SHT 4	PIO1_6-JOY_D	46	PIO1_6/ACMP_I2
SHT 4	PIO1_7-JOY_R	51	PIO1_7/ACMP3_I4
SHT 4	PIO1_8-JOY_L	53	PIO1_8/ACMP3_I3/SCT3_OUT4
SHT 4	PIO1_9-UART_RS485	54	PIO1_9/ACMP2_I4
SHT 2, 4	PIO1_10-RS485_RTS	59	PIO1_10/ACMP1_I4
	PIO1_11-ISP_1	38	PIO1_11

BOOT LOAD

KMR221GLFS SW2 — GND — NC NC — R65 100ohms — SJ7 — PIO1_10-RS485_RTS — PIO0_4-ADC0_4

U7 LQFP64 = 1-2
U7 LQFP48 = 2-3

WAKEUP

KMR221GLFS SW1 — GND — NC NC — +3.3V — R64 100Kohms — R63 100ohms — PIO0_17-OLED_EN

RGB LED

D8 — +3.3V

PIO0_1-SCT0_OUT4-BLUE — R62 270ohms — Blue

PIO0_24-SCT0_OUT6-GREEN — R60 270ohms — Green

PIO0_0-SCT0_OUT3-RED — R61 1.5Kohms — Red

LED_RGB_PLCC4

Solder bump jumpers
Default set by 0ohm resistor

U7 LQFP64 = 1-2
U7 LQFP48 = 2-3

SHT 4 CAN0_RD — SJ5 — PIO0_11-CAN_RD — PIO0_13-ISP_RX

SHT 4 CAN0_TD — SJ4 — PIO0_31-CAN_TD — PIO0_18-ISP_TX

SHT 2 TO_MUX_ISP_RX — SJ3 — PIO0_13-ISP_RX — PIO0_14

SHT 2, 4 ISP_TX — SJ2 — PIO0_18-ISP_TX — PIO0_15

SHT 4 ADC1_X — SJ6 — PIO0_16 — PIO0_11-CAN_RD

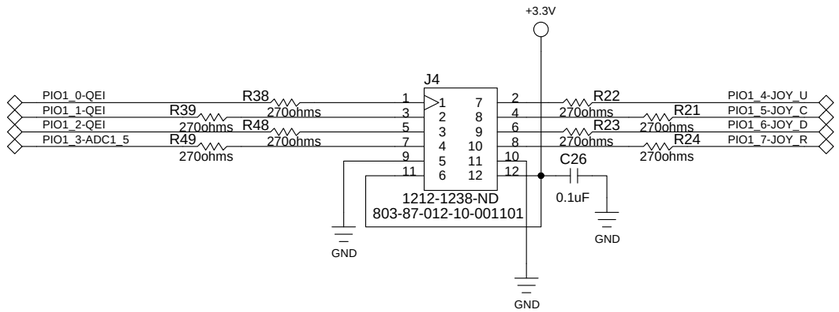
CONTRACT NO.		Target LPC1549	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	9/5/2013	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
ISSUED	9/05/13	www.standardics.nxp.com/microcontrollers/	
		SIZE D	FSCM NO.
		DWG. NO. Xpresso-LPC15xx	REV 9
		SCALE	SHEET 3 OF 04

H=8ND; V=4LA

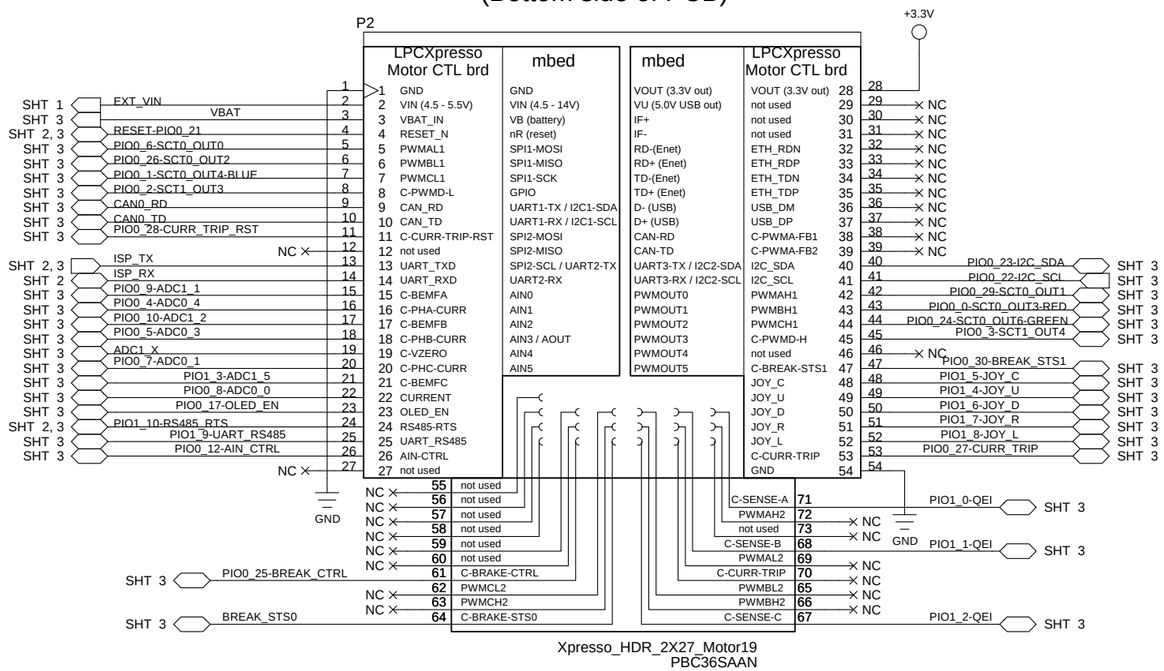
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

PMOD compatible header

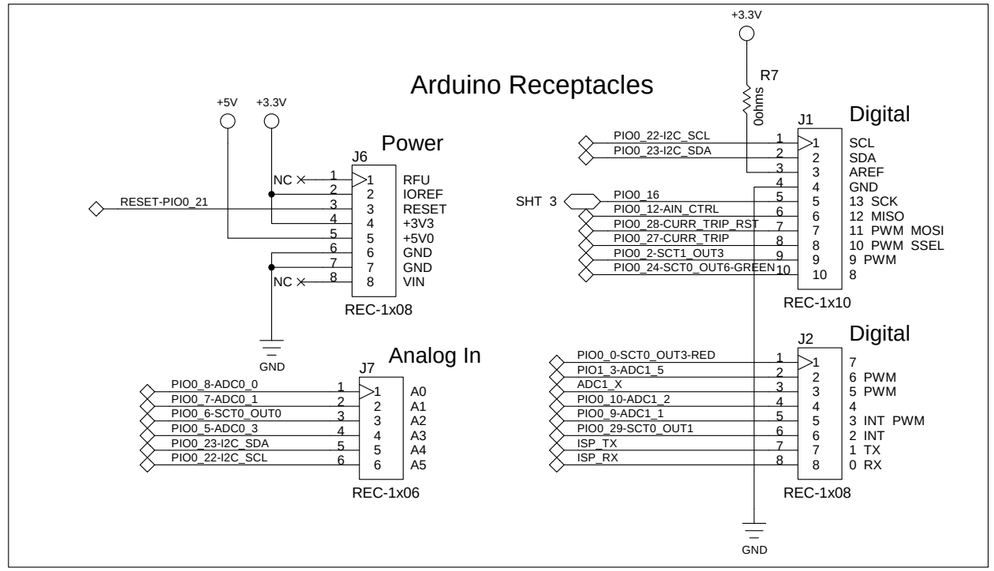


LPCXpresso Motor Control brd header (Bottom side of PCB)



Xpresso_HDR_2X27_Motor19
PBC36SAAN

Arduino Receptacles



CONTRACT NO.		Xpresso MC/Arduino/PMOD headers
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	9/5/2013	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	9/05/13	SIZE D | FSCM NO. | DWG. NO. Xpresso-LPC15xx | REV 9
		SCALE | SHEET 4 OF 04

H=8ND; V=4LA